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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/711,509

09/23/2004

Fang-Chen Luo

12405-US-PA-0P

5508

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01/20/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

BREWSTER, WILLIAM M

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/711,509

Applicant(s)

LUO ET AL.

Examiner

William M. Brewster

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8, 10 and 19-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10 and 19-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date. 010306.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8, 25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 8 and 25 specify a limitation for a difference in deposition rates for the amorphous layer. However, applicant's response received 4 January 2006 directly refutes this, stating that the deposition rates can vary. Applicant must withdraw the statements of 4 January 2006 or withdraw these claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 4, 8, 10, 19, 20, 22, 24, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al., US Patent No. 6,222,214 B1 in view of Lee et al., US Patent No. 6,737,305 B1.

Wu teaches, limitations from claim 1, a manufacturing method of a thin film transistor (TFT), comprising:

in fig. 6, forming a gate 14 over a substrate 10;
forming an inter-gate dielectric layer 16 over the substrate covering the gate;
forming a channel layer 18 over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer is or comprises a lightly doped amorphous silicon layer, col. 5, line 39 - col. 6, line 15, and
forming source/drain regions, part of 18, col. 5, lines 66 - col. 6, line 15, wherein the source/drain regions are separated by a distance;

limitations from claims 2, 20, the manufacturing method of claims 1, 19, wherein the channel layer comprises an N-type lightly doped amorphous silicon layer, col. 5, lines 39-56;

limitations from claim 4, 22, the method of claims 1, 19, wherein the channel layer is doped with phosphorus atoms at a concentration of phosphorous atoms is in the range of about $1\text{E}17 \text{ atom/cm}^3$ to about $1\text{E}18 \text{ atom/cm}^3$; about $1\text{E}16 \text{ atom/cm}^3$ to $1\text{E}18 \text{ atom/cm}^3$;

limitations from claim 10, 24, the manufacturing method of claims 1, 19, further comprising a step of forming, in fig. 7, a protection layer 22 over the substrate after the step of forming the source/drain regions covering the source/drain

regions, the channel layer and the inter-gate dielectric layer, col. 6, line 33 - col. 7, line 3.

Wuu does not specify forming source/drain region over the channel layer. While contacts for the source/drain regions are necessary for the device to be operational, Lee actually specifies it.

Lee teaches a manufacturing method of a thin film transistor (TFT), comprising: col. 4, line 54 - col. 5, line 61, in fig. 4A, forming a gate 102 over a substrate 100; in fig. 4B, forming an inter-gate dielectric layer 104 over the substrate covering the gate; in fig. 4C, forming a channel layer 106 over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer is or comprises a lightly doped amorphous silicon layer, col. 5, lines 4-18; and in fig. 4E, forming source/drain regions over the channel layer with ohmic contacts, the contacts and interconnects being regions of the source/drain features (not shown but describes) col. 5, lines 25-32, wherein the source/drain regions are separated by a distance;

limitations from claims 8, 25, the manufacturing method of claim 1, wherein the step of forming the channel layer comprises:

in fig. 4C, forming a first lightly doped sub-amorphous silicon layer 106A over the portion of the inter-gate dielectric layer at a first deposition rate (LDR, low deposition rate); and forming a second lightly doped sub-amorphous silicon layer 106B over the first lightly doped sub-amorphous silicon layer at a second

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deposition rate, (HDR, high deposition rate), wherein the first deposition rate is lower than the second deposition rate, col. 5, lines 4-18;

limitations from claim 9, the manufacturing method of claim 1, further comprising a step of forming, in fig. 4E an ohmic contact layer (not shown, but described) over the channel layer between the step of forming the channel layer and the step of forming the source/drain regions 108, col. 5, lines 25-32;

limitations from claim 19, further comprising a step of forming, in fig. 4E an ohmic contact layer (not shown, but described) over the channel layer, col. 5, lines 25-32.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 5-7, 21, 23, 26, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Lee as applied to claims 1, 2, 4, 8, 10, 19, 20, 22, 24, 25 above, and further in view of Yang et al., US Publication No. 2002/0102781 A1.

Lee teaches,

limitations from claims 6 and 7, the manufacturing method of claim 1; wherein the step of forming the channel layer comprises performing a chemical vapor

deposition (CVD) process using a reaction gas mixture comprising a silane (SiH_4), hydrogen (H_2), col. 5, lines 55-61.

Neither Wu nor Lee specifies using phosphine or boroethane, but Yang does. Yang teaches limitations from claims 3, 21 the manufacturing method of claim 1, 19, wherein the channel layer comprises a P-type lightly doped amorphous silicon layer; p. 2, ¶ 25; doping the amorphous silicon channel layer of the TFT with phosphine for an n-type TFT or boroethane for a p-type TFT, p. 2, ¶ 25;

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Yang's process with Lee's invention would have been beneficial because the well-known industry dopants are readily available and cost effective.

Neither Wu, Lee nor Yang specify for claims 5, 23, the concentration of the dopants, or claims 6, 7, 26, 27, the ratio of the reactants. However, the practitioner may optimize these ranges:

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More

particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.”

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmischer 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Whereas the doping concentrations maybe optimized by the practitioner, the claimed ranges are already well within the industry standard. Proffered as evidence only is Lee et al., US Publication No. 2004/0046171 A1. Lee (171) in figs. 4F and 4G, the active layer 41 is an amorphous silicon above substrate 40, and contains either phosphorus doping in the range of $1 \times 10^{11} \sim 1 \times 10^{22}$ ions/cm³ or boron doping in the range of $1 \times 10^{11} \sim 1 \times 10^{22}$ ions/cm³. As such ‘lightly doped’ is contained within a standard doping concentration.

Response to Arguments

Applicant's arguments filed 1 November 2005 have been fully considered but they are not persuasive. Applicant argues that Lee does not teach a lightly doped amorphous channel between the source/drain region.

Examiner has found Wu, which teaches a lightly doped amorphous region between the source and the drain regions. While Wu does not specify the source/drain regions are over the channel, Lee does specify contacts with interconnects over the source/drain region which are necessary for the Wu device to function.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. BREWSTER
PRIMARY EXAMINER

17 January 2006
WB